

# Formal Methods in Quantum Circuit Design

by

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# Formal Methods In Circuit Design

**Victoria Stavridou, Tom F.  
Melham, Raymond T. Boute**



## **Formal Methods In Circuit Design:**

*Formal Methods in Circuit Design* Victoria Stavridou,1993-07-22 Graduate level account of hardware verification and algebraic specification     **Theorem Provers in Circuit Design** Ramayya Kumar,Thomas Kropf,1995-03-06 This two volume set contains papers presented at the International Conference on Computational Engineering Science ICES 95 held in Mauna Lani Hawaii from 30 July to 3 August 1995 The contributions capture the state of the science in computational modeling and simulation in a variety of engineering disciplines civil mechanical aerospace materials and electronics engineering

**Correct Hardware Design and Verification Methods** Laurence Pierre,Thomas Kropf,2003-07-31 CHARME 99 is the tenth in a series of working conferences devoted to the development and use of leading edge formal techniques and tools for the design and verification of hardware and systems Previous conferences have been held in Darmstadt 1984 Edinburgh 1985 Grenoble 1986 Glasgow 1988 Leuven 1989 Torino 1991 Arles 1993 Frankfurt 1995 and Montreal 1997 This workshop and conference series has been organized in cooperation with IFIP WG 10.5 It is now the biannual counterpart of FMCAD which takes place every even numbered year in the USA The 1999 event took place in Bad Herrenalb a resort village located in the Black Forest close to the city of Karlsruhe The validation of functional and timing behavior is a major bottleneck in current VLSI design systems A predominantly academic area of study until a few years ago formal design and verification techniques are now migrating into industrial use The aim of CHARME 99 is to bring together researchers and users from academia and industry working in this active area of research Two invited talks illustrate major current trends the presentation by Gerard Berry Ecole des Mines de Paris Sophia Antipolis France is concerned with the use of synchronous languages in circuit design and the talk given by Peter Jansen BMW Munich Germany demonstrates an application of formal methods in an industrial environment The program also includes 20 regular presentations and 12 short presentations poster exhibitions that have been selected from the 48 submitted papers     *Automated Technology for Verification and Analysis* Zhiming Liu,Anders P. Ravn,2009-10-13 This book constitutes the proceedings of the 7th International Symposium on Automated Technology for Verification and Analysis ATVA 2009 held in Macao China in October 2009 The 23 regular papers and 3 tool papers presented together with 3 invited talks were carefully reviewed and selected from 74 research papers and 10 tool papers submissions The papers are organized in topical sections on state space reduction tools probabilistic systems model checking temporal logic abstraction and refinement and fault tolerant systems     *A Formal Approach to Hardware Design* Jørgen Staunstrup,2012-12-06 A Formal Approach to Hardware Design discusses designing computations to be realised by application specific hardware It introduces a formal design approach based on a high level design language called Synchronized Transitions The models created using Synchronized Transitions enable the designer to perform different kinds of analysis and verification based on descriptions in a single language It is for example possible to use exactly the same design description both for mechanically supported verification and synthesis Synchronized Transitions is supported by a

collection of public domain CAD tools These tools can be used with the book in presenting a course on the subject A Formal Approach to Hardware Design illustrates the benefits to be gained from adopting such techniques but it does so without assuming prior knowledge of formal design methods The book is thus not only an excellent reference it is also suitable for use by students and practitioners

*Digital System Verification* Lun Li, Mitchell Aaron Thornton, 2010 Integrated circuit capacity follows Moore's law and chips are commonly produced at the time of this writing with over 70 million gates per device Ensuring correct functional behavior of such large designs before fabrication poses an extremely challenging problem Formal verification validates the correctness of the implementation of a design with respect to its specification through mathematical proof techniques Formal techniques have been emerging as commercialized EDA tools in the past decade Simulation remains a predominantly used tool to validate a design in industry After more than 50 years of development simulation methods have reached a degree of maturity however new advances continue to be developed in the area A simulation approach for functional verification can theoretically validate all possible behaviors of a design but requires excessive computational resources Rapidly evolving markets demand short design cycles while the increasing complexity of a design causes simulation approaches to provide less and less coverage Formal verification is an attractive alternative since 100% coverage can be achieved however large designs impose unrealistic computational requirements Combining formal verification and simulation into a single integrated circuit validation framework is an attractive alternative This book focuses on an Integrated Design Validation IDV system that provides a framework for design validation and takes advantage of current technology in the areas of simulation and formal verification resulting in a practical validation engine with reasonable runtime After surveying the basic principles of formal verification and simulation this book describes the IDV approach to integrated circuit functional validation

*Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology* Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, 2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering

improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

*Theorem Provers in Circuit Design* Victoria Stavridou, Tom F. Melham, Raymond T. Boute, 1992 The papers in this volume address the role of mechanized theorem proving technology in the design of digital systems The primary focus is on the practical application of theorem provers to digital design rather than on theoretical foundations The diverse contributions include invited papers by the leading researchers Gordon and Hunt as well as technical contributions by many other prominent researchers in the field of machine assisted hardware verification This side of the Proceedings reflects current research activity and the section containing tutorial papers on several influential theorem provers serves as an introduction to this exciting field

Optimization Methods in Electronic Circuit Design R. E. Massara, 1991 Principally aimed at degree level students of electronic engineering this book assesses the application of optimization theory to engineering and suggests that it offers the prospect of solutions to problems for which no formal design methods exist

**CONCUR '98 Concurrency Theory** Davide Sangiorgi, Robert de Simone, 1998-08-19 This book constitutes the refereed proceedings of the 9th International Conference on Concurrency Theory CONCUR 98 held in Nice France in September 1998 The 35 revised full papers presented were carefully selected from a total of 104 submissions Also presented are five invited contributions Among the topics covered are moduls of computation and semantic domains process algebras Petri Nets event structures real time systems hybrid systems model checking verification techniques refinement rewriting typing systems and algorithms etc

**Dependable Computing for Critical Applications 4** Flaviu Cristian, Gerard LeLann, Teresa Lunt, 2012-12-06 This volume contains the articles presented at the Fourth International FIP Working Conference on Dependable Computing for Critical Applications held in San Diego California on January 4 6 1994 In keeping with the previous three conferences held in August 1989 at Santa Barbara USA in February 1991 at Tucson USA and in September 1992 at Mondello Italy the conference was concerned with an important basic question can we rely on computer systems for critical applications This conference like its predecessors addressed various aspects of dependability a broad term defined as the degree of trust that may justifiably be placed in a system s reliability availability safety security and performance Because of its broad scope a main goal was to contribute to a unified understanding and integration of these concepts The Program Committee selected 21 papers for presentation from a total of 95 submissions at a September meeting in Menlo Park California The resulting program represents a broad spectrum of interests with papers from universities corporations and government agencies in eight countries The selection process was greatly facilitated by the diligent work of the program committee members for which we are most grateful As a Working Conference the program was designed to promote the exchange of ideas by extensive discussions All paper sessions ended with a 30 minute discussion period on the topics covered by the session In addition three panel sessions have been organized

**Formal Methods in Quantum Circuit Design** Matthew Amy, 2019

The design and compilation of correct efficient quantum circuits is integral to the future operation of quantum computers. This thesis makes contributions to the problems of optimizing and verifying quantum circuits with an emphasis on the development of formal models for such purposes. We also present software implementations of these methods which together form a full stack of tools for the design of optimized formally verified quantum oracles. On the optimization side we study methods for the optimization of Rz and CNOT gates in Clifford Rz circuits. We develop a general efficient optimization algorithm called phase folding which reduces the number of Rz gates without increasing any metrics by computing its phase polynomial. This algorithm can further be combined with synthesis techniques for CNOT dihedral operators to optimize circuits with respect to particular costs. We then study the optimal synthesis problem for CNOT dihedral operators from the perspectives of Rz and CNOT gate optimization. In the case of Rz gate optimization we show that the optimal synthesis problem is polynomial time equivalent to minimum distance decoding in certain Reed Muller codes. For the CNOT optimization problem we show that the optimal synthesis problem is at least as hard as a combinatorial problem related to Gray codes. In both cases we develop heuristics for the optimal synthesis problem which together with phase folding reduces T counts by 42% and CNOT counts by 22% across a suite of real world benchmarks. From the perspective of formal verification we make two contributions. The first is the development of a formal model of quantum circuits with ancillary bits based on the Feynman path integral along with a concrete verification algorithm. The path integral model with some syntactic sugar further doubles as a natural specification language for quantum computations. Our experiments show some practical circuits with up to hundreds of qubits can be efficiently verified. Our second contribution is a formally verified optimizing compiler for reversible circuits. The compiler compiles a classical irreversible language to reversible circuits with a formal machine checked proof of correctness written in the proof assistant F. The compiler is structured as a partial evaluator allowing verification to be carried out significantly faster than previous results.

**Designing Correct Circuits** Geraint Jones, Mary Sheeran, 1991. These proceedings contain the papers presented at a workshop on Designing Correct Circuits jointly organised by the Universities of Oxford and Glasgow and held in Oxford on 26-28 September 1990. There is a growing interest in the application to hardware design of the techniques of software engineering. As the complexity of hardware systems grows and as the cost both in money and time of making design errors becomes more apparent so there is an eagerness to build on the success of mathematical techniques in program development. The harsher constraints on hardware designers mean both that there is a greater need for good abstractions and rigorous assurances of the trustworthiness of designs and also that there is greater reason to expect that these benefits can be realised. The papers presented at this workshop consider the application of mathematics to hardware design at several different levels of abstraction. At the lowest level of this spectrum Zhou and Hoare show how to describe and reason about synchronous switching circuits using UNILY a formalism that was developed for reasoning about parallel programs. Aagaard and Leeser use standard mathematical tech

niques to prove correct their implementation of an algorithm for Boolean simplification The circuits generated by their formal synthesis system are thus correct by construction Thuau and Pilaud show how the declarative language LUSTRE which was designed for program ming real time systems can be used to specify synchronous circuits [Formal Methods and Models for System Design](#) Rajesh Gupta,Paul Le Guernic,Sandeep Kumar Shukla,Jean-Pierre Talpin,2004-06-30 Perhaps nothing characterizes the inherent heterogeneity in embedded systems than the ability to choose between hardware and software implementations of a given system function Indeed most embedded systems at their core represent a careful division and design of hardware and software parts of the system To do this task effectively models and methods are necessary functionality to capture application behavior needs and system implementation constraints Formal modeling can be valuable in addressing these tasks As with most engineering domains co design practice defines the state of the it seeks to add new capabilities in system conceptualization mod art though eling optimization and implementation These advances particularly those related to synthesis and verification tasks directly depend upon formal understanding of system behavior and performance measures Current practice in system modeling relies upon exploiting high level programming frameworks such as SystemC Esterel to capture design at increasingly higher levels of abstraction and attempts to reduce the system implementation task While raising the abstraction levels for design and verification tasks to be really useful these approaches must also provide for reuse adaptation of the existing intellectual property IP blocks [Formal System Verification](#) Rolf Drechsler,2017-06-21 This book provides readers with a comprehensive introduction to the formal verification of hardware and software World leading experts from the domain of formal proof techniques show the latest developments starting from electronic system level ESL descriptions down to the register transfer level RTL The authors demonstrate at different abstraction layers how formal methods can help to ensure functional correctness Coverage includes the latest academic research results as well as descriptions of industrial tools and case studies [Correct Hardware Design and Verification Methods](#) ,1995 **Research in Engineering and Applied Science at Cornell University** ,1989 **Symbolic Simulation Methods for Industrial Formal Verification** Robert B. Jones,2012-12-06 Symbolic Simulation Methods for Industrial Formal Verification contains two distinct but related approaches to the verification problem Both are based on symbolic simulation The first approach is applied at the gate level and has been successful in verifying sub circuits of industrial microprocessors with tens and even hundreds of thousands of gates The second approach is applied at a high level of abstraction and is used for high level descriptions of designs The book contains three main topics Self consistency a technique for deriving a formal specification of design behavior from the design itself The use of the parametric representation to encode predicates as functional vectors for symbolic simulation an important step in addressing the state explosion problem Incremental flushing a method used to verify high level descriptions of out of order execution Symbolic Simulation Methods for Industrial Formal Verification concludes with work on verification of simplified models of out of order

processors     Switching Circuits and Systems J. E. O'Brien, M. Raspanti, 1955\*  
*Reports* ,1982-07

*Scientific and Technical Aerospace*

## **Formal Methods In Circuit Design** Book Review: Unveiling the Magic of Language

In an electronic era where connections and knowledge reign supreme, the enchanting power of language has become more apparent than ever. Its power to stir emotions, provoke thought, and instigate transformation is truly remarkable. This extraordinary book, aptly titled "**Formal Methods In Circuit Design**," published by a highly acclaimed author, immerses readers in a captivating exploration of the significance of language and its profound effect on our existence. Throughout this critique, we shall delve into the book's central themes, evaluate its unique writing style, and assess its overall influence on its readership.

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### **Formal Methods In Circuit Design Introduction**

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