Hardware-Software Co-Synthesis of Distributed Embedded Systems

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Hardware Software Co Synthesis Of Distributed Embedded Systems

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Hardware Software Co Synthesis Of Distributed Embedded Systems:

   Hardware-Software Co-Synthesis of Distributed Embedded Systems Ti-Yen Yen,Wayne Wolf,2013-11-11 Embedded computer systems use both off the shelf microprocessors and application specific integrated circuits ASICs to implement specialized system functions Examples include the electronic systems inside laser printers cellular phones microwave ovens and an automobile anti lock brake controller Embedded computing is unique because it is a co design problem the hardware engine and application software architecture must be designed simultaneously Hardware Software Co Synthesis of Distributed Embedded Systems proposes new techniques such as fixed point iterations phase adjustment and separation analysis to efficiently estimate tight bounds on the delay required for a set of multi rate processes preemptively scheduled on a real time reactive distributed system Based on the delay bounds a gradient search co synthesis algorithm with new techniques such as sensitivity analysis priority prediction and idle processing elements elimination are developed to select the number and types of processing elements in a distributed engine and determine the allocation and scheduling of processes to processing elements New communication modeling is also presented to analyze communication delay under interaction of computation and communication allocate interprocessor communication links and schedule communication Hardware Software Co Synthesis of Distributed Embedded Systems is the first book to describe techniques for the design of distributed embedded systems which have arbitrary hardware and software topologies The book will be of interest to academic researchers for personal libraries and advanced topics courses in co design as well as industrial designers who are building high performance real time embedded systems with multiple processors   Co-Synthesis of Hardware and Software for Digital Embedded Systems Rajesh Kumar Gupta,2012-09-27 Co Synthesis of Hardware and Software for Digital Embedded Systems with a Foreword written by Giovanni De Micheli presents techniques that are useful in building complex embedded systems These techniques provide a competitive advantage over purely hardware or software implementations of time constrained embedded systems Recent advances in chip level synthesis have made it possible to synthesize application specific circuits under strict timing constraints This work advances the state of the art by formulating the problem of system synthesis using both application specific as well as reprogrammable components such as off the shelf processors Timing constraints are used to determine what part of the system functionality must be delegated to dedicated application specific hardware while the rest is delegated to software that runs on the processor This co synthesis of hardware and software from behavioral specifications makes it possible to realize real time embedded systems using off the shelf parts and a relatively small amount of application specific circuitry that can be mapped to semi custom VLSI such as gate arrays The ability to perform detailed analysis of timing performance provides the opportunity of improving the system definition by creating better phototypes Co Synthesis of Hardware and Software for Digital Embedded Systems is of interest to CAD researchers and developers who want to branch off into the expanding field of hardware software co design as well as to digital system

designers who are interested in the present power and limitations of CAD techniques and their likely evolution **Readings in Hardware/Software Co-Design** Giovanni De Micheli,Rolf Ernst,Wayne Wolf,2002 This title serves as an introduction ans reference for the field with the papers that have shaped the hardware software co design since its inception in the early 90s

Fourth International Workshop on Hardware/Software Co-Design, Codes/CASHE '96 Donald E. Thomas,Rolf Ernst,1996 Embedded architecture co synthesis and system integration B Lin S Vercauteren and H De Man A multi level transformation approach to HW SW codesign a case study T K Y Cheung G Hellestrand and P Kanthamanon Fully parallel hardware software codesign for multi dimensional DSP applications M Sheliga N L Passos and E H M Sha A co design methodology based on formal specification and high level estimation C Carreras and others Speed up estimation for HW SW systems W Hardt and W Rosenstiel A framework for interactive analysis of timing constraints in embedded systems R K Gupta The interplay of run time estimation and granularity in HW SW partitioning J Henkel and R Ernst Partitioning and exploration strategies in the TOSCA co design flow A Balboni W Fornaciari and D Sciuto Process partitining for distributed embedded systems J Hou and W Wolf Two level partitioning of image processing algorithms for the parallel map oriented machine R W Hartenstein J Becker and R Kress PACE a dynamic programming algorithm for hardware software partitioning P V Knudsen and J Madsen A model for the coanalysis of hardware and software architectures F Rose and others A case study in co design of communication controllers R Gerndt Formal verification of embedded systems based on CFSM networks F Balarin and others Towards a model for hardware and software functional partitioning F Vahid and T dm Le Implications of codesign as a natural constituent of a systems engineering discipline for computer based systems M Voss and O Hammerschmidt Uninterpreted co simulation for performance evaluation of HW SW systems J P Calvez D Heller and O Pasquier Fast and accurate hardware software co simulation using software timing estimates C Passerone and others

Hardware/software Co-design of Heterogeneous Real-time Distributed Embedded Systems Bharat Purushottam Dave,1998 **Hardware/Software Co-Design for Data Flow Dominated Embedded Systems** Ralf Niemann,1998-10-31 Introduces different tasks of hardware software co design including system specification hardware software partitioning co synthesis and co simulation Summarizes and classifies co design tools and methods for these tasks and presents the co design tool COOL useful for solving co design tasks for the class of data flow dominated embedded systems Primary emphasis is on hardware software partitioning and the co synthesis phase and their coupling A mathematical formulation of the hardware software partitioning problem is given and several novel approaches are presented and compared for solving the partitioning problem Annotation copyrighted by Book News Inc Portland OR *Proceedings of the ... International Symposium on Hardware/Software Codesign* ,2002 39th Power Sources Conference ,2000 13th Symposium on Integrated Circuits and Systems Design Ricardo Augusto da Luz Reis,Jose Carlos Monteiro,Wilhelmus Van Noije,2000 These papers are taken from 13th Brazilian Symposium on Integrated Circuit Design SBCCI 2000 They address issues such as

microarchitectures architecture logic design analogue design high level synthesis digital design physical modelling reconfigurable hardware and more   Proceedings of the Fifth International Workshop on Hardware/Software Co-Design (Codes/CASHE '97) ,1997 Contains papers from the March 1997 workshop in sections on scheduling and allocation target architectures and debugging optimization communication issues synthesis of run time environments modeling and simulation acceleration and trading off hardware and software Topics include interface optimization during hardware software partitioning software architecture synthesis for retargetable real time embedded systems software acceleration using coprocessors and an evolutionary approach to system level synthesis No index Annotation copyrighted by Book News Inc Portland OR   *Proceedings, ... International Symposium on VLSI Design* ,2003   **DETC2005** ,2005   High Performance Computing ,2002   **Digest of Technical Papers** ,2001   **Proceedings** ,1995   Proceedings of ASP-DAC/VLSI Design 2002 ,2002 Papers from a January 2002 conference are organized into four sessions each on low power design synthesis testing layout and interconnects and technology as well as two sessions each on embedded systems verification and VLSI architecture one session on analog design and one session on hot c   **ASICON 2003** Ting-Ao Tang,2003   *Proceedings of the ASP-DAC ... Asia and South Pacific Design Automation Conference* ,2002   *Annales des télécommunications* ,2004   IEEE International Conference on Electronics, Circuits and Systems ,1999

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